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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/766,117	01/27/2004	Yauo-Nan Wang	WANG, Yauo-Nan ET AL./BA-	2111

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BUCKNAM AND ARCHER
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EXAMINER	
KRAMSKAYA, MARINA	
ART UNIT	**PAPER NUMBER**
2858	

DATE MAILED: 06/13/2005

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/766,117	WANG ET AL.	
	Examiner	Art Unit	
	Marina Kramskaya	2858	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☐ Responsive to communication(s) filed on _____.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) 1-3 is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) 1-3 is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☒ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on 27 January 2004 is/are: a)☐ accepted or b)☒ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☒ All b)☐ Some * c)☐ None of:

1.☒ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

Drawings

1. The drawings are objected to under 37 CFR 1.83(a). The drawings must show every feature of the invention specified in the claims. Therefore, the voltage of the impedance test apparatus, as in claim 2, must be shown or the feature(s) canceled from the claim(s). No new matter should be entered.

Corrected drawing sheets in compliance with 37 CFR 1.121(d) are required in reply to the Office action to avoid abandonment of the application. Any amended replacement drawing sheet should include all of the figures appearing on the immediate prior version of the sheet, even if only one figure is being amended. The figure or figure number of an amended drawing should not be labeled as "amended." If a drawing figure is to be canceled, the appropriate figure must be removed from the replacement sheet, and where necessary, the remaining figures must be renumbered and appropriate changes made to the brief description of the several views of the drawings for consistency. Additional replacement sheets may be necessary to show the renumbering of the remaining figures. Each drawing sheet submitted after the filing date of an application must be labeled in the top margin as either "Replacement Sheet" or "New Sheet" pursuant to 37 CFR 1.121(d). If the changes are not accepted by the examiner, the applicant will be notified and informed of any required corrective action in the next Office action. The objection to the drawings will not be held in abeyance.

2. Figure 2 should be designated by a legend such as --Prior Art-- because only that which is old is illustrated. See MPEP § 608.02(g). Corrected drawings in compliance with 37 CFR 1.121(d) are required in reply to the Office action to avoid abandonment of the application. The replacement sheet(s) should be labeled "Replacement Sheet" in the page header (as per 37 CFR 1.84(c)) so as not to obstruct any portion of the drawing figures. If the changes are not accepted by the examiner, the applicant will be notified and informed of any required corrective action in the next Office action. The objection to the drawings will not be held in abeyance.

Specification

3. The disclosure is objected to because of the following informalities: grammatical and spelling errors appear throughout the specification as well as the claims.

Appropriate correction is required.

Claim Objections

4. Claims 1-2 are objected to because of the following informalities: the term "DC impedance" is not a term generally accepted in the art. An impedance value is generally an AC quantity including a resistance and a reactance values. "DC impedance" is considered to be a DC resistance only.

Appropriate correction is required.

5. Claim 1 is objected to because of the following informalities: it is unclear which units are outputting "outputting different source signals". Only the output of the high voltage signal is disclosed. Appropriate correction is required.

6. Claim 2 objected to because of the following informalities: it is unclear how the voltage is provided to the impedance test apparatus. Appropriate correction is required.

7. Claim 2 is objected to because of the following informalities: the term "subtracted" in line 6 of claim 2 should be "subtract". Appropriate correction is required.

8. Claims 1 & 3 are objected to because of the following informalities: the preamble "a floating-impedance high voltage simultaneously test" is grammatically incorrect. The following change is suggested: "A floating-impedance and high voltage simultaneous testing" method or circuit.

Appropriate correction is required.

9. Claim 3 is objected to because of the following informalities: "said controller" in line 3 of page 10, lacks antecedent basis. Appropriate correction is required.

Claim Rejections - 35 USC § 112

10. The following is a quotation of the first paragraph of 35 U.S.C. 112:

> The specification shall contain a written description of the invention, and of the manner and process of making and using it, in such full, clear, concise, and exact terms as to enable any person skilled in the

> art to which it pertains, or with which it is most nearly connected, to make and use the same and shall set forth the best mode contemplated by the inventor of carrying out his invention.

11. Claim 2 is rejected under 35 U.S.C. 112, first paragraph, as failing to comply with the enablement requirement. The claim(s) contains subject matter which was not described in the specification in such a way as to enable one skilled in the art to which it pertains, or with which it is most nearly connected, to make and/or use the invention.

It is unclear how the voltage in the DC impedance test apparatus is generated. Further, claim 1 set forth a limitation for a "low voltage DC impedance"; however, claim 2 requires a "voltage higher that the maximum voltage generated by said high voltage generation means". Therefore, it is unclear how a low voltage DC impedance measurement can be obtained by a test apparatus supplying a higher voltage that that of the high voltage generator.

Claim Rejections - 35 USC § 102

12. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

13. Claims 1 & 3 are rejected under 35 U.S.C. 102(b) as being anticipated by Allfather, US 5,818,245.

As per Claim 1, Allfather discloses a floating-impedance and high voltage simultaneous testing method, characterized in that using two or more sets of conditions capable of simultaneously outputting different source signals (column 2, lines 63-65) to perform simultaneously the high voltage test (column 5, lines 47-50) and DC impedance test (low voltage DC impedance is broadly interpreted as a DC resistance; column 6, lines 35-37), in which conducting a DC impedance test via a floating DC impedance electric meter (FIG's 1-2) at the same time of conducting high voltage safety test via a high voltage generation means (high voltage DC power supply **93**), that is conducting synchronized tests of safety (column 6, lines 4-9) and DC impedance on electric parts or products (column 1, lines 5-7).

As per Claim 3, Allfather discloses a floating-impedance high voltage simultaneously test circuit, for conducting simultaneously safety test on primary coil (column 1, lines 39-40) and case of a testing object, comprises:

- a high voltage generation means (high voltage DC power supply **93**) for generation of a required test voltage for safety test for the testing object;
- a current detection means (column 7, lines 21-25) for detecting current generated by said high voltage generation means by flowing through the testing object;
- a floating impedance test means (FIG's 1-2; column 1, lines 5-7) for measuring the floating impedance of the primary coil or thermal filament of the testing object (i.e. specimen such as a winding: column 1, lines 39-40) ;

- a isolation means **129** for isolating (column 6, lines 43-44) a controller (processor **73**) unit from said floating impedance test means to conduct a impedance test by said impedance test means under a floating mode;
- a control unit for controlling (processor **73**) the operation of above means; wherein by using a combined circuit constituted of above means, said high voltage generation means (high voltage DC power supply **93**) generates a high voltage required by a high voltage test to conduct a test on a testing object, and determines good/failure (column 1, line 13) of a product with current value read by said current detection means (column 7, lines 21-25); at the same time, a control signal is sent from said controller unit to said floating impedance test means via the isolation means **129** for conducting a impedance test, while test data measured by said floating impedance test means is returned to said controller unit via said isolation means.

Conclusion

14. The prior art made of record and not relied upon is considered pertinent to applicant's disclosure. Bald et al., US 6,054,865, discloses a high voltage and impedance test system and method with a leakage current measurement function. Stahl, US 5,537,044, discloses a system and method of performing a high voltage test and a floating impedance test on a winding.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Marina Kramskaya whose telephone number is (571)272-2146. The examiner can normally be reached on M-F 7:00-4:00.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Edward Lefkowitz can be reached on (571)272-2180. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

MK

ANJAN DEB
PRIMARY EXAMINER

Marina Kramskaya
Examiner
Art Unit 2858